

REMARKS

No claims have been amended herein. Claims 1-9 have been canceled as being directed to a non-elected invention. Applicants reserve the right to file a divisional application at a later date capturing the subject matter recited in claims 1-9 canceled herein. Claims 10-23 remain pending in the captioned case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Section 103 Rejection

Claims 10 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,144,624 to Sharper et al. (hereinafter “Sharper”) in view of U.S. Patent No. 4,893,310 to Robertson et al. (hereinafter “Robertson”). Claims 11-17 and 19-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sharper, Robertson, and U.S. Patent No. 6,782,066 to Nicholas et al. (hereinafter “Nicholas”).

To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. See *In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03. Specifically, “all words in a claim must be considered when judging the patentability of that claim against the prior art.” *In re Wilson* 424 F.2d., 1382 (CCPA 1970). Using these standards, Applicant contends that the cited art fails to teach or suggest all features of the currently pending claims, some distinctive features of which are set forth in more detail below.

The combination of Sharper and Roberson do not teach or suggest a comparator that replaces first signal bits within a first data sequence with second signal bits within a second data sequence if the first signal bits differ from the second signal bits. Present independent

claims 10 and 18 each describe a comparator or “comparing” step. The comparator or comparing step compares first signal bits within a first data sequence with second signal bits within a second data sequence. If the result of that comparison yields a difference between the first signal bits and the second signal bits, then the first signal bits are replaced by the second signal bits. Replacement occurs by substituting the second bits into the locations of the first signal bits contained within the first data sequence. In this manner, the signal bits are constantly updated, but only if a change occurs. If the comparison does not yield a difference, then replacement does not occur and the digital signal processor is not notified through an interrupt or any other processing stall functionality.

Contrary to independent claims 10 and 18, it is impossible for Sharper or Robertson to perform any replacement whatsoever. Instead, Sharper describes a signaling bit detection circuit 100 (Sharper -- Fig. 4). The detection circuit 100 detects whether a logic 1 or logic 0 is present in the eighth bit location of every frame (Sharper -- col. 5, lines 35-49; Fig. 3). The incoming frames are placed into a shift register 142 via line 40, with clock 41 serially clocking each frame bit-by-bit into shift register 142 (Sharper -- col. 5, lines 59-67). The eighth bit of every frame is read from shift register 142 and placed into comparator 45 (Sharper -- Fig. 4). Depending on the logic state of the logically compared eighth bit, comparator 45 will produce an output that notes whether the system mode is in an “on-hook” or “off-hook” condition (Sharper -- col. 5, lines 44-57; col. 6 lines 3-16). Processor 50 can interpret comparator 45 output to generate a signal that corresponds either to an on-hook or an off-hook mode (Sharper -- col. 6, lines 17-19).

While comparator 45 compares the logic states of signaling bits placed in the eighth bit position of each frame, nowhere in Sharper is there any mention that a signaling bit (or any bit) is replaced as a result of that comparison. Certainly there is no mention in Sharper that if the eighth signaling bit within the first frame is different from the eighth signaling bit within the second frame, that somehow the eighth signaling bit within the first frame is replaced with the eighth signaling bit within the second frame. In fact, to do so would defeat the entire purpose of Sharper which is to maintain the signaling bit status to note whether the mode is on-hook or off-hook. The mechanism for formulating the system mode status in Sharper does not derive from any comparison function, much less from comparator 45. Instead, comparator 45 simply detects on-hook or off-hook, but does not replace signaling bits to change the system mode status. When reviewing Sharper, a skilled

artisan would know that a significant difference exists between detection and replacement and would further know that the output of comparator 45 does not control, modify, replace, or substitute first signal bits with second signal bits as presently claimed.

The shortcomings of Sharper are compounded in Robertson. Robertson makes no mention whatsoever of replacing first signal bits with second signal bits. Instead, Robertson only describes detection of any occurrence of matches. Again, detection is not the same as replacement, and certainly would not be interpreted to be the same by a skilled artisan.

Sharper and Roberson do not teach or suggest a comparator that notifies a digital signal processor of a replacement. Present claim 10 not only describes a comparator that replaces first signal bits with second signal bits, but also a comparator that notifies a digital signal processor (DSP) of that replacement. In this fashion, the DSP need only be notified if a change exists. If a change does not occur, then the DSP is not bothered using standard interrupts or any other process halting function.

Contrary to present claim 10, Sharper makes no mention of any notification to a DSP as recognized by the Examiner on page 2 of the Office Action. However, the Examiner believes that Robertson describes a system for notifying a DSP. The Examiner points to member 882 in Robertson for performing a comparison and the result of that comparison is then somehow forwarded to a DSP (Office Action -- page 2). Applicants respectfully disagree. First, the comparator function 882 has no means whatsoever for communicating the comparison output to a processor since all functional arrows extend inward to comparator 882, not outward from comparator 882 (Robertson -- Fig. 12). Thus, the comparator apparatus 882 cannot signal anything whatsoever to a DSP through processor buffer 805 or otherwise. Second, even if comparator 882 could hypothetically forward a signal to a DSP, it only determines an occurrence of matches (Robertson -- col. 16, lines 51-55). Nowhere in Robertson is there any mention that comparator apparatus 882 does anything other than determining the occurrence of matches “in combination with instruction of central processor origin and signals from detectors 815-817 . . .” (Robertson -- col. 16, lines 53-55). Determining the occurrence of matches is quite different from notifying a DSP of a replacement as presently claimed.

For at least the foregoing reasons, Applicant asserts that independent claims 10 and 18, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, Applicants respectfully request removal of this rejection.

CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed August 7, 2006. In view of the remarks herein, Applicant asserts that pending claims 10-23 are in condition for allowance. If the Examiner has any questions, comments or suggestions, the undersigned earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 12-2252.

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